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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER
WANG, ALBERT C

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/894,294	NALAWADI	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to the amendment filed March 29, 2005.

2. Applicant's arguments with respect to claims 1-29 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 8, 12, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Herzi, U.S. Patent No. 6,615,288.

As per claim 1, Herzi teaches a system comprising:

a processor coupled to a bus (fig. 2, CPU 201);

a memory coupled to the bus (fig. 2, memory 203);

an external bus controller coupled to the bus (fig. 1, USB controller; fig. 2; col. 5, 24-35); and

a basic input-output system (BIOS) coupled to the bus (fig. 2, BIOS 202; fig. 4; col. 5, lines 36-52), the BIOS comprising an external bus support component to cause a periodic interrupt to be generated and to provide support for external bus enabled devices responsive to the interrupt (figs. 3 & 5; col. 6, lines 34-46).

As per claim 2, Herzi teaches the external bus support component is to provide support for external bus enabled devices until an operating system providing external bus support is loaded (col. 1, line 66 – col. 2, line 20; col. 7, lines 10-15).

As per claim 3, Herzi teaches the external bus enabled devices comprise at least one of a keyboard, a mouse, a floppy drive, a biometric device, a hard disk drive, a compact disk read-only memory (CD-ROM) player (fig. 2).

As per claim 4, Herzi teaches the system wherein:

the external bus controller is a Universal Serial Bus (USB) host controller (fig. 2; claim 7);

the external bus support component is a USB support component (fig. 4); and

the external bus enabled devices are USB devices (fig. 2; claim 8).

As per claim 8, Herzi teaches a system comprising:

a processor coupled to a bus (fig. 2, CPU 201);

a memory coupled to the bus (fig. 2, memory 203);

an external bus controller coupled to the bus (fig. 1, USB controller; fig. 2; col. 5, 24-35);

an external bus enabled device coupled to the external bus controller (fig. 1, USB keyboard, USB mouse);

a basic input-output system (BIOS) coupled to the bus (fig. 2, BIOS 202; fig. 4; col. 5, lines 36-52), the BIOS having instructions which when executed cause the processor to perform operations comprising:

obtaining a portion of the memory to be used to maintain a plurality of external bus device data (col. 5, lines 36-45; col. 6, lines 16-33);

causing an interrupt to be periodically generated (figs. 3 & 5; col. 6, lines 34-46); and

handling input produced by the external bus enabled device using the portion of the memory responsive to the interrupt (figs. 3 & 5).

As per claim 12, Herzi teaches the system wherein:

the external bus controller is a Universal Serial Bus (USB) host controller (fig. 2; claim 7);

the external bus support component is a USB support component (fig. 4); and

the external bus enabled device is a USB device.

As per claim 14, Herzi teaches a method comprising:

obtaining a portion of a memory to be used to maintain a plurality of USB device data (figs. 2 & 4; col. 5, lines 36-45; col. 6, lines 16-33);

causing an interrupt to be periodically generated by an external bus support component (figs. 3 & 5; col. 6, lines 34-46); and

handling input produced by one or more USB devices using the portion of the memory (figs. 3 & 5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 24 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi, U.S. Patent No. 6,615,288.

As per claim 24, Herzi teaches a method having a processor perform operations comprising:

obtaining a portion of a memory to be used to maintain a plurality of external bus device data (figs. 2 & 4; col. 5, lines 36-45; col. 6, lines 16-33);

causing an interrupt to be periodically generated (figs. 3 & 5; col. 6, lines 34-46); and

handling input produced by an external bus enabled device using the portion of the memory responsive to the interrupt (figs. 3 & 5).

However, while Herzi teaches a BIOS firmware (fig. 2, BIOS 202), Herzi does not expressly teach a machine readable medium having instructions for the updating of BIOS to support the method steps above. Official Notice is taken that using a machine readable medium for "re-flashing" of flash ROM to provide an updated version of BIOS is well known in the art (for example see Gharda et al., U.S. Patent No. 6,560,702, col. 1, lines 53-65). At the time of the invention, it would have been obvious to one of ordinary skill in the art that "re-flashing" is common practice for updating BIOS code.

As per claim 28, Herzi teaches the system wherein:

the external bus controller is a Universal Serial Bus (USB) host controller (fig. 2; claim 7);

the external bus support component is a USB support component (fig. 4); and

the external bus enabled device is a USB device.

5. Claims 6, 7, 9, 11, 15, 17, 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi, as applied to claims 1, 8, 14 and 24 above, and further in view of Chaiken, U.S. Patent No. 6,128,732.

As per claims 6, 7, 9, 15 and 25, Herzi teaches that the processor has a system management mode (col. 4, lines 26-34), but does not expressly teach that the processor conforms to the 32 bit Intel Architecture (IA-32). Chaiken teaches that Intel processors with 32 bit architecture have a system management mode. At the time of the invention, it would have been obvious to one of ordinary skill in the art that Chaiken's IA-32 is applicable to Herzi's processor, as IA-32 is well known in the art. Herzi teaches the periodic interrupt is a system management interrupt (SMI) (fig. 3, step 303).

As per claims 11, 17 and 27, Chaiken teaches de-allocating a portion of memory when the operating system is loaded (col. 1, line 60 – Col. 2, line 5).

6. Claims 5, 13, 18 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi/Chaiken, as applied to claims 6, 7, 9, 11, 15, 17, 25 and 27 above, and further in view of Intel, "Instantly Available Power Managed Desktop PC Design Guide", Revision 1.2, September 25, 1998 ("Intel").

As per claim 5, Chaiken teaches adherence to the ACPI Specification (col. 5, lines 8-13 & 56-64), but does not expressly teach details of memory mapping and BIOS with regards to the ACPI specification and the BIOS comprises a software component to implement the ACPI

specification. Intel teaches such details (sec. 4, ACPI BIOS design considerations). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Intel's ACPI implementation to Herzi/Chaiken's system. A motivation for doing so would have been to facilitate power management (Intel, sec. 1.1).

As per claims 13, 18 and 29, Intel teaches a non-volatile-sleeping (NVS) memory region (sec. 4.2.2, ACPI Non-Volatile-Sleeping Memory).

7. Claims 10, 16 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi/Chaiken as applied to claims 8, 14, and 24 above, and further in view of Abgrall, U.S. Patent No. 6,401,202.

As per claims 10, 16 and 26, Herzi does not expressly teach the details of disabling the periodically generated interrupt when an operating system providing external bus device support is completely loaded. Abgrall teaches disabling an interrupt once a task has been completed (Fig. 6, step 650). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Abgrall's disabling an interrupt to Herzi's system. A motivation for doing so would have been to ensure the integrity of the system.

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi as applied to claim 14 above, and further in view of Eichler, Jr. et al., U.S. Patent No. 6,772,252 ("Eichler").

As per claim 20, Chaiken teaches removing code from memory when the code is no longer necessary (col. 1, line 60 – col. 2, line 5), but does not expressly teach determining

whether an operating system providing USB device support is loaded. Eichler teaches determining whether an operating system provides USB support (fig. 7, step 704). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Eichler's determining to Herzi's method. A motivation for doing so would have been to determine when code is no longer necessary.

9. Claims 19, 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi as applied to claim 14 above, and Herzi/Eichler as applied to claim 20 above, and further in view of Intel Corporation, "Universal Host Controller Interface (UHCI) Design Guide", Revision 1.1, March 1996 ("UHCI").

As per claim 19, Herzi does not teach the details of USB data transfer. UHCI teaches control transfers to one or more USB devices using the portion of the memory (sec. 1.1, Data transfer types; sec. 1.2, schedule constructed in host memory; fig. 4, example schedule). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply UHCI's control transfers to Herzi's method, so as to use a USB defined transfer type.

As per claim 21, UHCI teaches checking a frame list base address register value to determine whether it is set to the address of the portion of the memory (fig. 3; secs. 1.2.1 & 1.4.1).

As per claim 23, UHCI teaches adjusting the frame bandwidth of interrupt transfers based on data traffic involving the one or more USB devices (sec. 1.3, Scheduling). Consequently the rate of the interrupt is adjusted.

10. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Herzi as applied to claim 14 above, and further in view of "Universal Serial Bus PC Legacy Compatibility Specification", Draft Revision 0.9, May 30, 1996 ("USBLegacy").

As per claim 22, Herzi does not expressly teach disabling of USB legacy support. USBLegacy teaches the step of disabling when transitioning from legacy mode support to extrinsic mode (sec. 4.1.1-3; sec. 6.1.1). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply the specification of USBLegacy to the Herzi's method, as the specification is well known in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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June 13, 2005

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100